WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor substrate;

a plurality of isolation regions in the semiconductor substrate that define an active region;

a gate electrode on the active region, wherein the gate electrode comprises a metal silicide layer on a polysilicon layer; and

a conductive layer that is on, and electrically connected to, the gate electrode;

wherein the conductive layer bridges at least one gap in the metal silicide layer.

2. The semiconductor device of Claim 1, wherein the conductive layer is directly on the metal silicide layer.

3. The semiconductor device of Claim 1, further comprising a gate insulation pattern between the active region and the gate electrode.

4. The semiconductor device of Claim 1, wherein the conductive layer is a conductive line pattern.

5. The semiconductor device of Claim 4, wherein the conductive line pattern is formed of at least one of aluminum, tungsten, titanium, tantalum, or copper.

6. The semiconductor device of Claim 4, further comprising an interlayer dielectric on the semiconductor substrate, and wherein the conductive line pattern is disposed in a groove in the interlayer dielectric.

7. The semiconductor device of Claim 6, wherein the interlayer dielectric includes a second groove, and wherein the device further comprises a plug line that electrically connects a source/drain region in the semiconductor device with a source/drain region of an adjacent semiconductor device.

8. The semiconductor device of Claim 1, further comprising a planarized interlayer dielectric on the semiconductor substrate, wherein the top surface of the planarized interlayer dielectric and the top surface of the gate electrode are substantially the same height above the semiconductor substrate.

9. The semiconductor device of Claim 1, further comprising a second active region in the semiconductor substrate with a second gate electrode thereon, wherein the second gate electrode comprises a metal silicide layer on a polysilicon layer, and wherein the conductive layer is a conductive line pattern that electrically connects the gate electrode and the second gate electrode.

10. The semiconductor device of Claim 9, wherein the conductive line pattern is directly on both the gate electrode and the second gate electrode.

11. The semiconductor device of Claim 1, wherein the conductive layer decreases the resistance of the gate electrode.

12. A semiconductor device comprising:

a semiconductor substrate;

a gate line including a gate insulation pattern and a gate electrode which are sequentially stacked on the semiconductor substrate;

a spacer formed on a sidewall of the gate line; and

a conductive line pattern disposed on the gate line; and

wherein the conductive line pattern is parallel to the gate line and electrically connected to the gate electrode.

13. The semiconductor device of Claim 12, wherein the gate electrode comprises a doped polysilicon layer.

14. The semiconductor device of Claim 13, further comprising a metal silicide layer, wherein the metal silicide layer is on the doped polysilicon layer.

15. The semiconductor device of Claim 14, further comprising an interlayer dielectric on the semiconductor substrate that includes a groove that exposes a top surface of the gate line, and wherein the conductive line pattern is provided in the groove.

16. The semiconductor device of Claim 15, further comprising an etch-stop layer between the semiconductor substrate and the interlayer dielectric, wherein the etch-stop layer has an etch selectivity with respect to the interlayer dielectric.

17. The semiconductor device of Claim 12, further comprising an interlayer dielectric which is formed on the semiconductor substrate that is planarized down to a top surface of the gate line.

18. The semiconductor device of Claim 12, wherein the conductive line pattern has at least the same length as the gate line.

19. The semiconductor device of Claim 12, wherein the conductive line pattern is made of metal.

20. The semiconductor device of Claim 14, wherein the conductive layer bridges at least one gap in the metal silicide layer.

21. The semiconductor device of Claim 12, wherein the conductive layer decreases the resistance of the gate electrode.

22. A semiconductor device comprising:

a semiconductor substrate;

a first gate line and a second gate line on the semiconductor substrate and spaced apart from each other, the first gate line including a first gate electrode stacked on a first gate insulation pattern, and the second gate line including a second gate electrode stacked on a second gate insulation pattern; and

a conductive line pattern on the first and second gate lines, wherein the conductive line pattern has a first portion parallel to the first gate line and a second portion parallel to the second gate line, and wherein the conductive line pattern electrically connects the first and second gate electrodes with each other.

23. The semiconductor device of Claim 22, wherein the first and second gate lines comprise a doped polysilicon layer.

24. The semiconductor device of Claim 23, wherein the first and second gate lines further comprise a metal silicide layer on the doped polysilicon layer.

25. The semiconductor device of Claim 22, further comprising a spacer disposed on a sidewall of the first and second gate lines and an interlayer dielectric covering the semiconductor substrate that includes a groove that exposes top surfaces of the first and second gate line; and

wherein the conductive line pattern is disposed in the groove in the interlayer dielectric.

26. The semiconductor device of Claim 25, further comprising an etch-stop layer between the semiconductor substrate and the interlayer dielectric, wherein the etch-stop layer has an etch selectivity with respect to the interlayer dielectric.

27. The semiconductor device of Claim 22, further comprising an interlayer dielectric on the semiconductor substrate that is planarized to the height of the first and second gate lines.

28. The semiconductor device of Claim 22, wherein the first portion of the conductive line pattern is at least the same length as the first gate line, and the second portion of the conductive line pattern is at least the same length as the second gate line.

29. The semiconductor device of Claim 22, wherein the conductive line pattern is made of metal.

30. The semiconductor device of Claim 24, wherein the conductive layer bridges at least one gap in the metal silicide layer.

31. The semiconductor device of Claim 22, wherein the conductive layer decreases the resistance of the gate electrode.

32. A method of forming a semiconductor device, comprising:

forming a gate line that comprises at least a gate insulation pattern and a gate electrode on a semiconductor substrate;

forming a spacer on a sidewall of the gate line;

forming an interlayer dielectric on the semiconductor substrate, the spacer and the gate line;

exposing a top surface of the gate line; and

forming a conductive line pattern on the exposed gate line that is parallel to the gate line.

33. The method of Claim 32, wherein the gate electrode comprises at least a polysilicon layer.

34. The method of Claim 33, wherein the gate electrode further comprises a metal silicide layer, and wherein the metal silicide layer is formed on the doped polysilicon layer.

35. The method of Claim 32, wherein exposing the top surface of the gate line comprises patterning the interlayer dielectric to form a groove that exposes the top surface of the gate line, and wherein forming the conductive line pattern comprises forming a conductive layer on the entire surface of the semiconductor substrate to fill the groove and then planarizing the conductive layer down to a top surface of the interlayer dielectric to form the conductive line pattern in the groove.

36. The method of Claim 35, wherein the method further comprises:

forming an etch-stop layer on the entire surface of a semiconductor substrate including the spacer before formation of the interlayer dielectric wherein the etch-stop layer has an etch selectivity with respect to the interlayer dielectric;

patterning the etch-stop layer above the gate line after patterning the interlayer dielectric to expose the top surface of the gate line.

37. The method of Claim 32, wherein exposing the top surface of the gate line comprises planarizing the interlayer dielectric until the top surface of the gate line is exposed and wherein forming the conductive line pattern comprises forming a conductive layer on the semiconductor substrate and the exposed the gate line and then patterning the conductive layer to form the conductive line pattern on the gate line.

38. The method of Claim 32, wherein the conductive line pattern is made of metal.

39. A method of forming a semiconductor device, comprising:

forming a first gate line and a second gate line that is spaced apart from the first gate line on a semiconductor substrate, the first gate line including a first gate electrode stacked on a first gate insulation pattern, and the second gate line including a second gate electrode stacked on a second gate insulation pattern;

forming a spacer on a sidewall of the first and second gate lines;

forming an interlayer dielectric on the semiconductor substrate and the spacer;

exposing a top surface of the first gate line and a top surface of the second gate line; and

forming a conductive line pattern on the exposed top surfaces of the first and second gate lines, wherein the conductive line pattern electrically connects the first electrode to the second gate electrode.

40. The method of Claim 39, wherein the first and second gate electrodes each include a doped polysilicon layer.

41. The method of Claim 40, wherein the first and second gate electrodes each further include a metal sdilicide layer on the doped polysilicon layer.

42. The method of Claim 39, wherein exposing the top surface of the gate line and forming the conductive line pattern comprise:

patterning the interlayer dielectric to form a groove that exposes top surfaces of the first and second gate lines;

forming a conductive layer on the surface of the semiconductor substrate to fill the groove; and

planarizing the conductive layer down to a top surface of the interlayer dielectric to form the conductive line pattern in the groove.

43. The method of Claim 42, wherein the method further comprises:

forming an etch-stop layer on an entire surface of the semiconductor substrate before formation of the interlayer dielectric, wherein the etch-stop layer has an etch selectivity with respect to the interlayer dielectric; and

patterning the etch-stop layer after patterning the interlayer dielectric to expose the top surface of the gate line.

44. The method of Claim 39, wherein exposing the top surface of the gate line comprises planarizing the interlayer dielectric until the top surfaces of the first and second gate lines are exposed, and wherein forming the conductive line pattern comprises forming a conductive layer on the semiconductor substrate and the exposed

first and second gate lines and then patterning the conductive layer to form the conductive line pattern on the top surfaces of the first and second gate lines.

45. The method of Claim 39, wherein the conductive line pattern is made of metal.